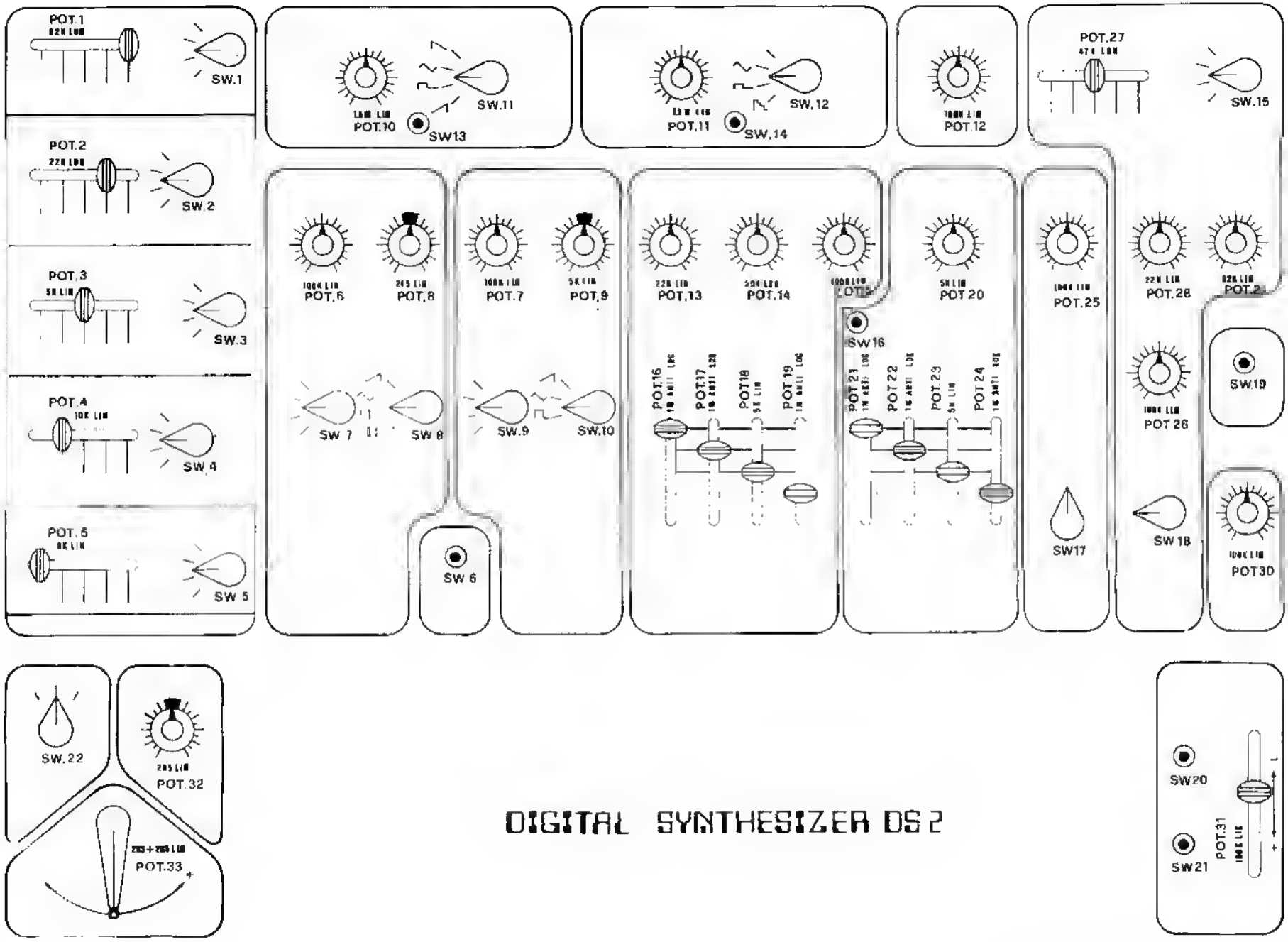
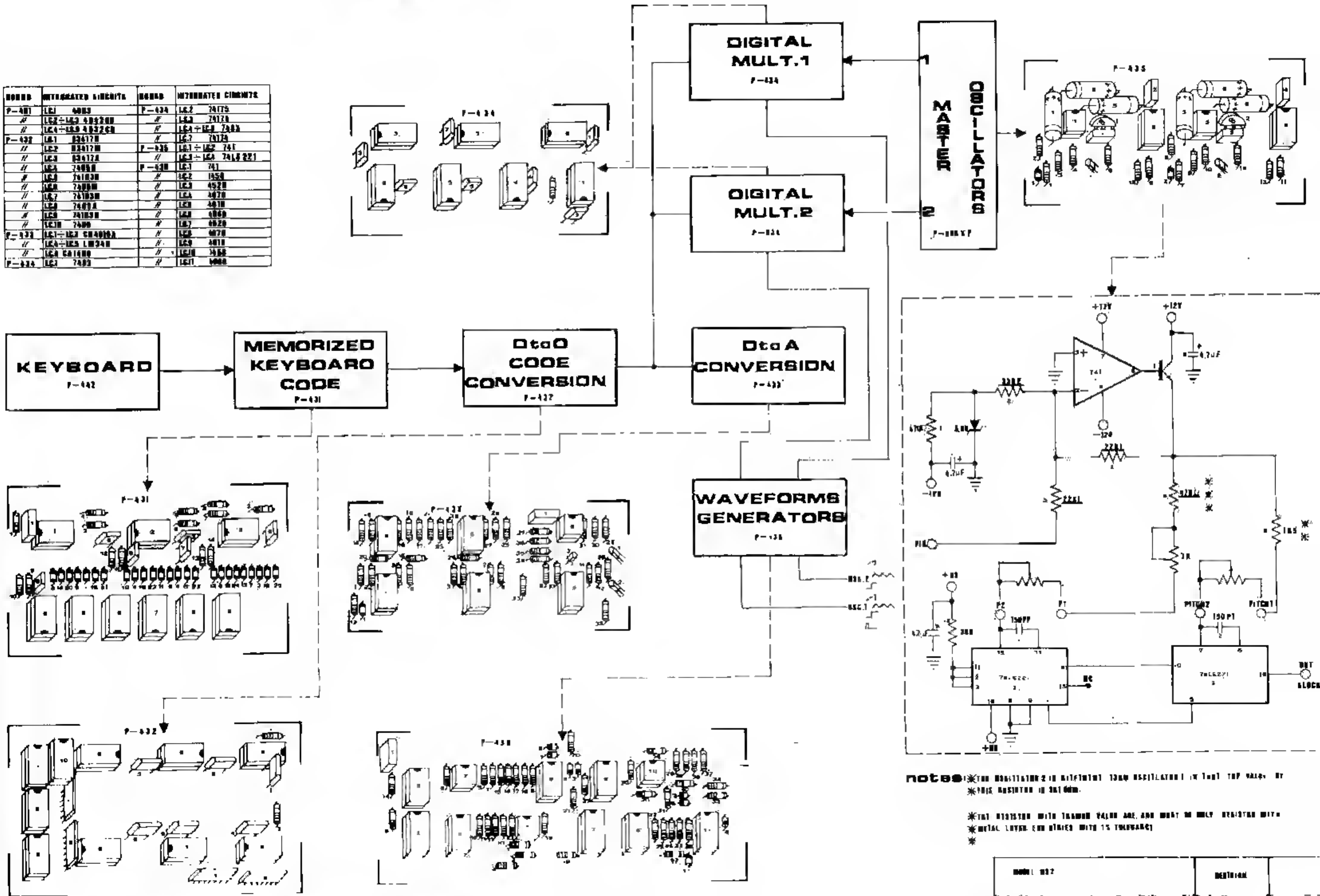


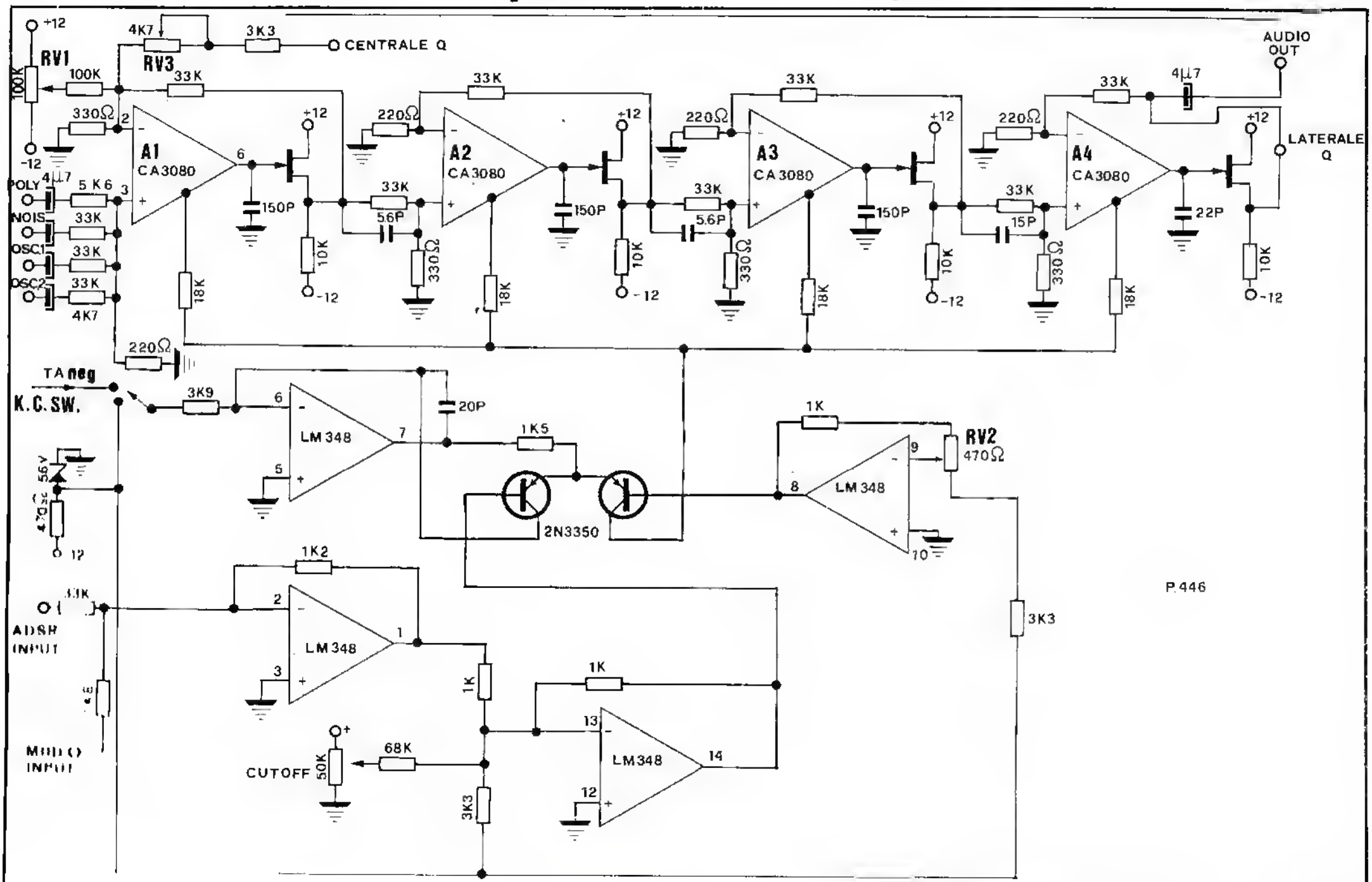
DIGITAL SYNTHESIZER DS 2

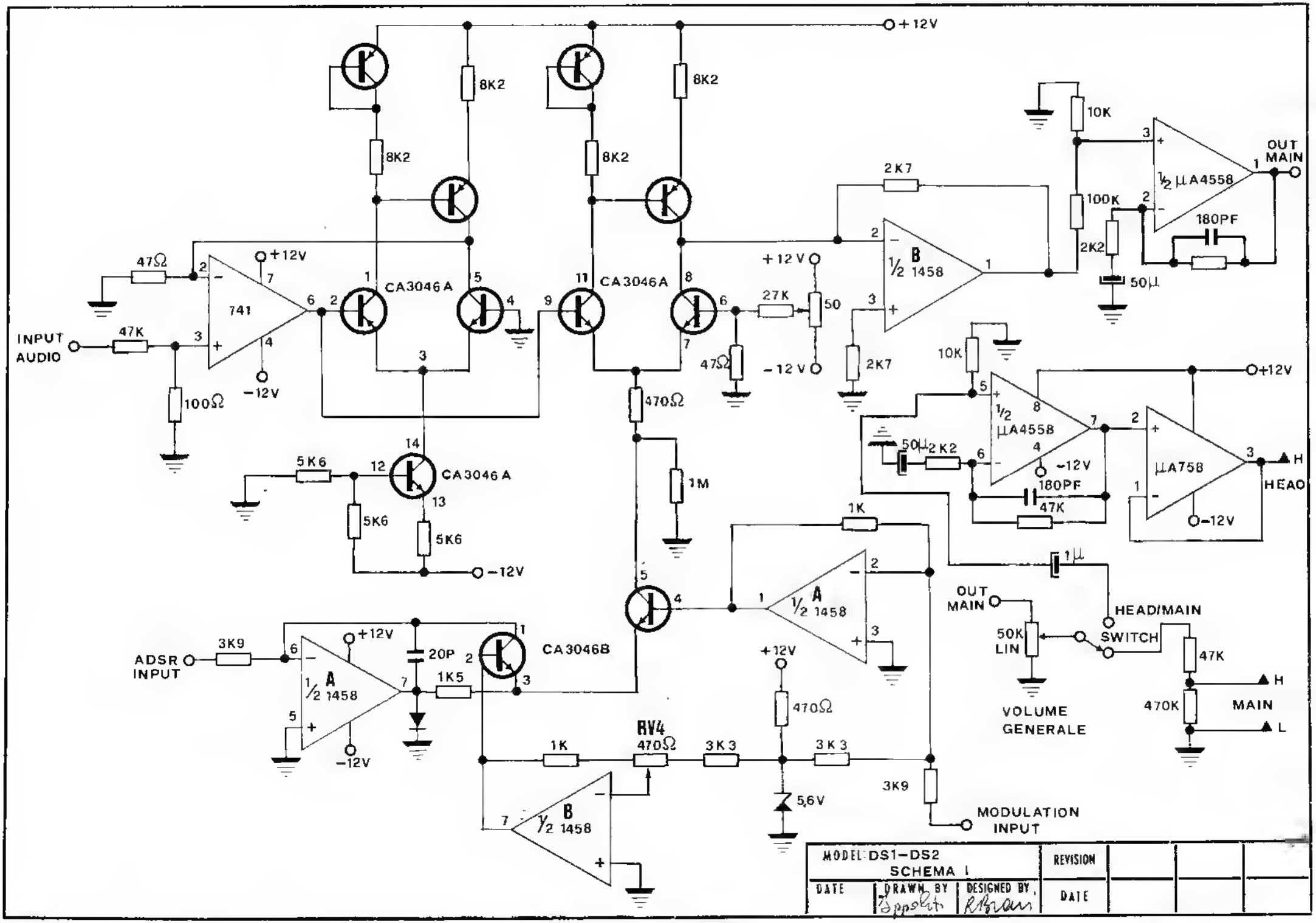


BOARD	INTEGRATED CIRCUITS	BOARD	INTEGRATED CIRCUITS
P-431	IC1 [illegible]	P-434	IC2 74175
//	IC2÷IC3 [illegible]	//	IC3 [illegible]
//	IC4÷IC9 [illegible]	//	IC4÷IC6 [illegible]
P-432	IC1 [illegible]	//	IC7 [illegible]
//	IC2 [illegible]	P-435	IC1÷IC2 741
//	IC3 [illegible]	//	IC3÷IC4 74LS221
//	IC4 [illegible]	P-436	IC1 741
//	IC5 [illegible]	//	IC2 [illegible]
//	IC6 [illegible]	//	IC3 4520
//	IC7 [illegible]	//	IC4 [illegible]
//	IC8 [illegible]	//	IC5 [illegible]
//	IC9 [illegible]	//	IC6 [illegible]
//	IC10 [illegible]	//	IC7 [illegible]
P-433	IC1÷IC3 [illegible]	//	IC8 [illegible]
//	IC4÷IC5 [illegible]	//	IC9 [illegible]
//	IC6 [illegible]	//	IC10 [illegible]
P-434	IC1 [illegible]	//	IC11 [illegible]

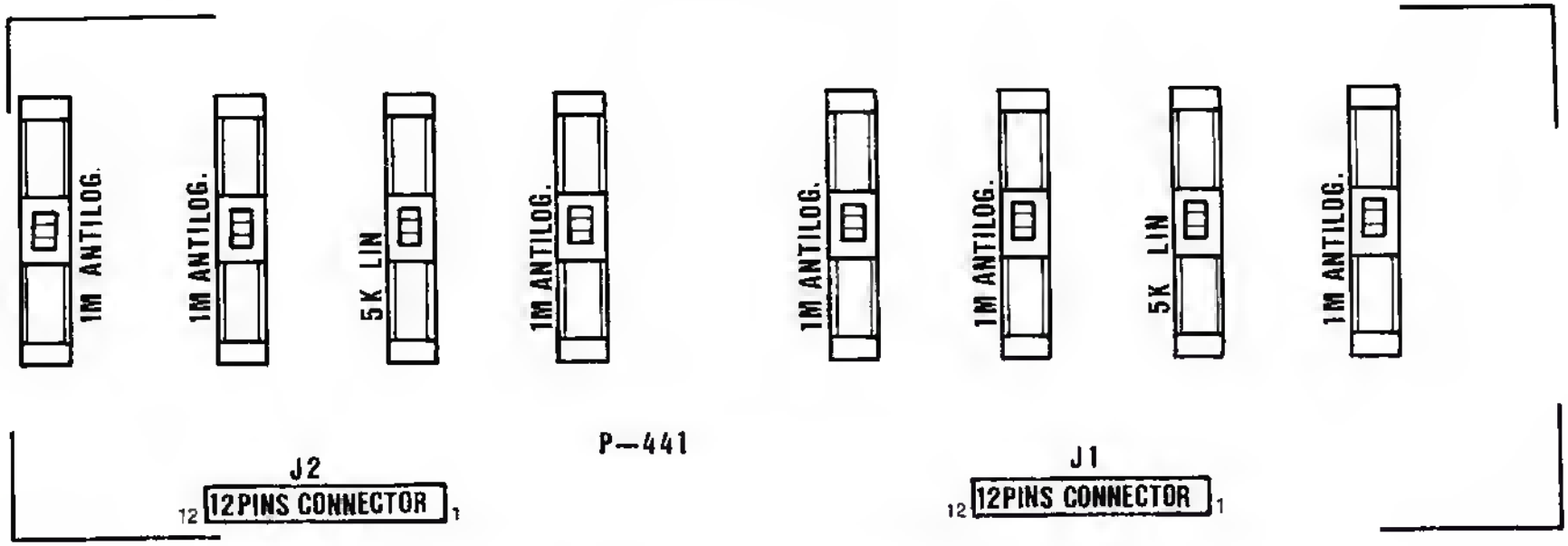
notes: [illegible]

MODEL [illegible]			DESTINATION
SCALE [illegible]	DRAWN BY [illegible]	DESIGNED BY [illegible]	DATE


+12
RV1
100K
100K
-12
4K7
RV3
3K3
CENTRALE Q
33K
330Ω
A1
CA3080
150P
10K
-12
33K
56P
330Ω
18K
220Ω
A2
CA3080
A3
CA3080
A4
CA3080
22P
15P
4µ7
AUDIO OUT
LATERALE Q
POLY
NOIS
OSC1
OSC2
5 K6
4K7
TA neg
K.C.SW.
3K9
20P
LM 348
1K5
2N3350
1K
RV2
470Ω
1K2
ADSR INPUT
MIDI INPUT
CUTOFF
50K
68K
3K3
P.446
DWG3
MODEL DS1–DS2
SCHEMA H
REVISION
DATE
DRAWN BY
DESIGNED BY
DATE


+12V
8K2
8K2
8K2
8K2
10K
OUT MAIN
½ µA4558
100K
180PF
2K2
50µ
2K7
½ B 1458
+12V
27K
50
-12V
47Ω
CA3046A
CA3046A
741
47Ω
+12V
INPUT AUDIO
47K
100Ω
-12V
470Ω
1M
5K6
CA3046A
5K6
5K6
-12V
2K7
10K
½ µA4558
50µ
2K2
180PF
47K
-12V
µA758
+12V
H
HEAD
1K
1µ
OUT MAIN
50K LIN
VOLUME GENERALE
HEAD/MAIN SWITCH
47K
470K
H
MAIN
L
ADSR INPUT
3K9
+12V
20P
CA3046B
1K5
½ A 1458
-12V
+12V
470Ω
RV4 470Ω
1K
3K3
3K3
5,6V
3K9
MODULATION INPUT
½ B 1458
MODEL: DS1-DS2
SCHEMA I
REVISION
DATE
DRAWN BY
DESIGNED BY
DATE

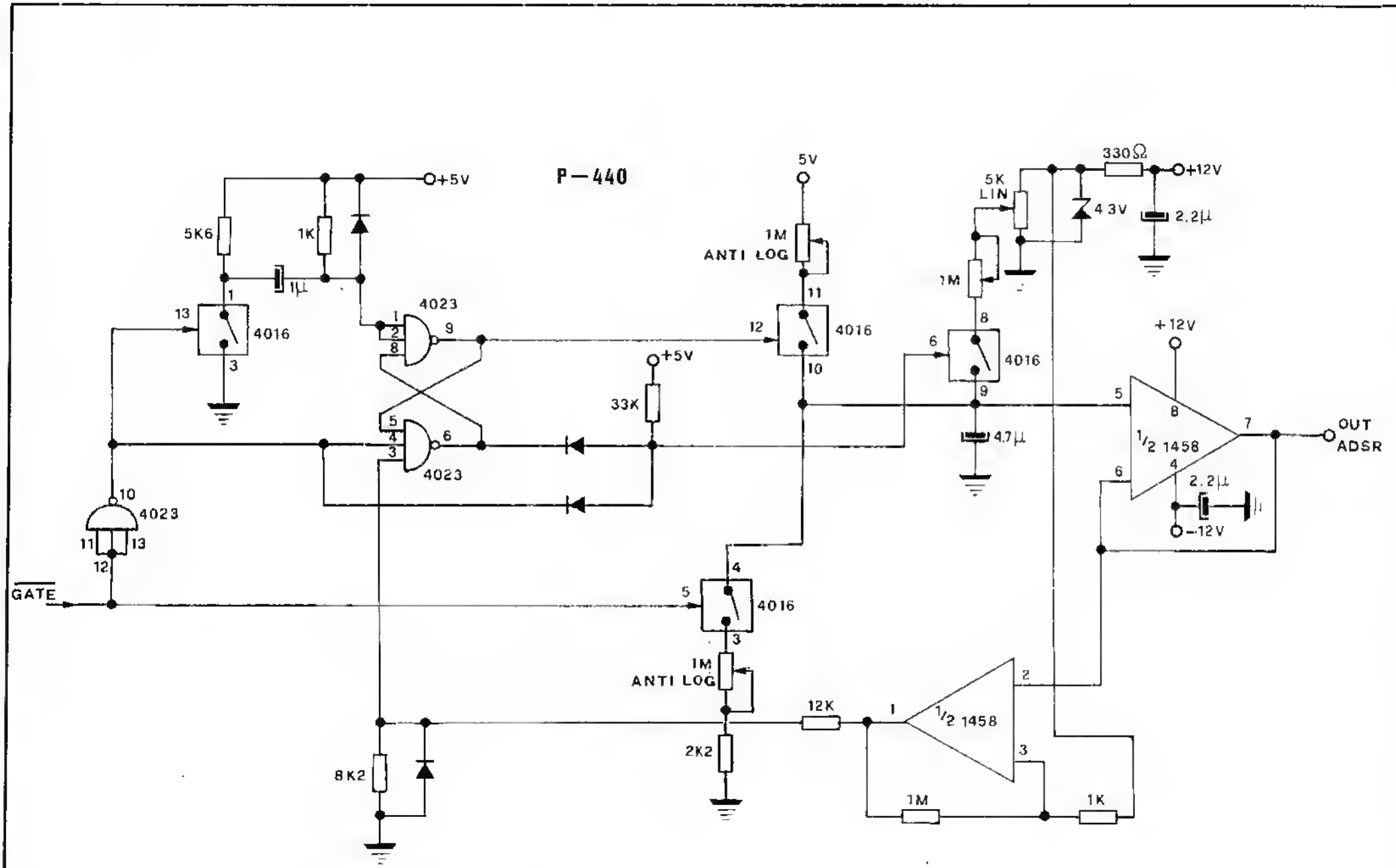
DWG4



DWG8

PIN	REFERENCE J2	PIN	REFERENCE J1
1	OUT AOSR VCF	1	+12V
2	" " "	2	−12V
3	" " "	3	R POT.
4	+5V	4	S POT.
5	R POT.	5	GND
6	S POT.	6	"
7	GND	7	"
8	"	8	"
9	"	9	D POT.
10	"	10	A POT.
11	D POT.	11	GATE
12	A POT.	12	OUT ADSR VCA

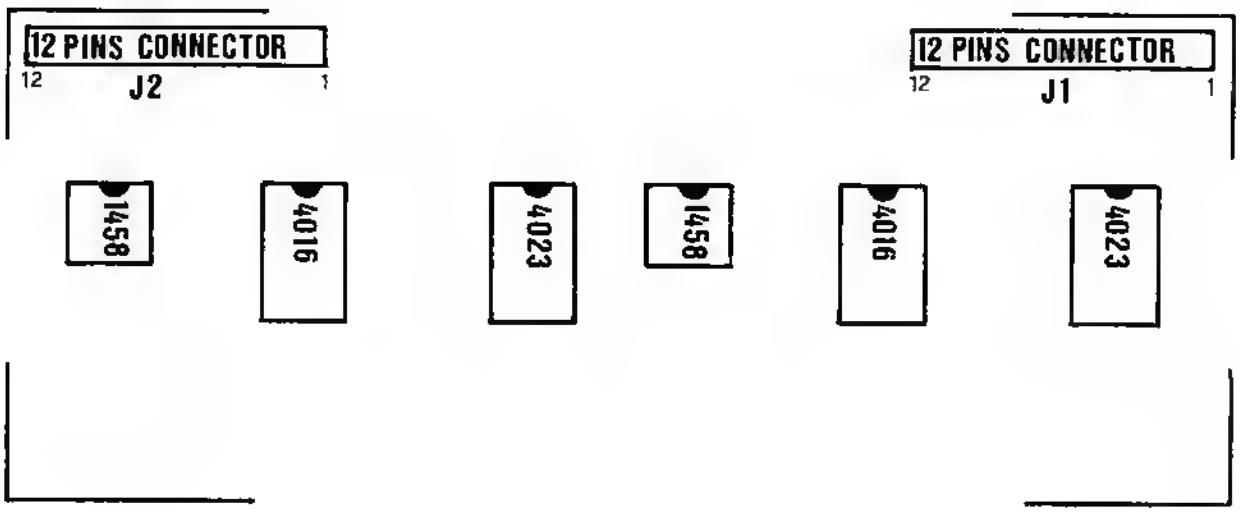
MODEL DS2 SCHEMA 1			REVISION		
DATE	DRAWN BY	DESIGNED BY	DATE		



MODEL DS1—DS2 SCHEMA L			REVISION			
DATE	DRAWN BY Appolot	DESIGNED BY R Bran	DATE			

DWG6

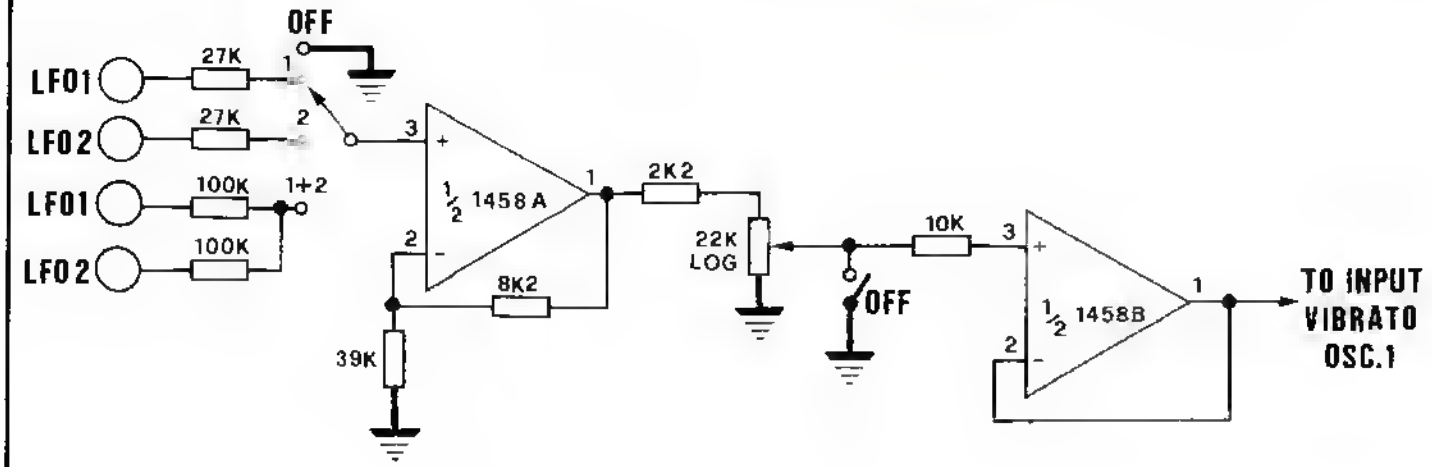
P.440

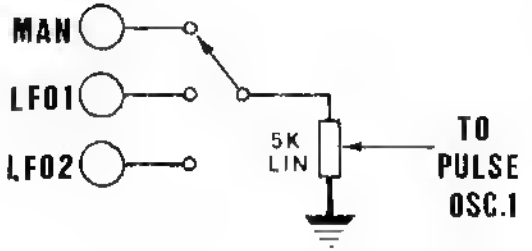


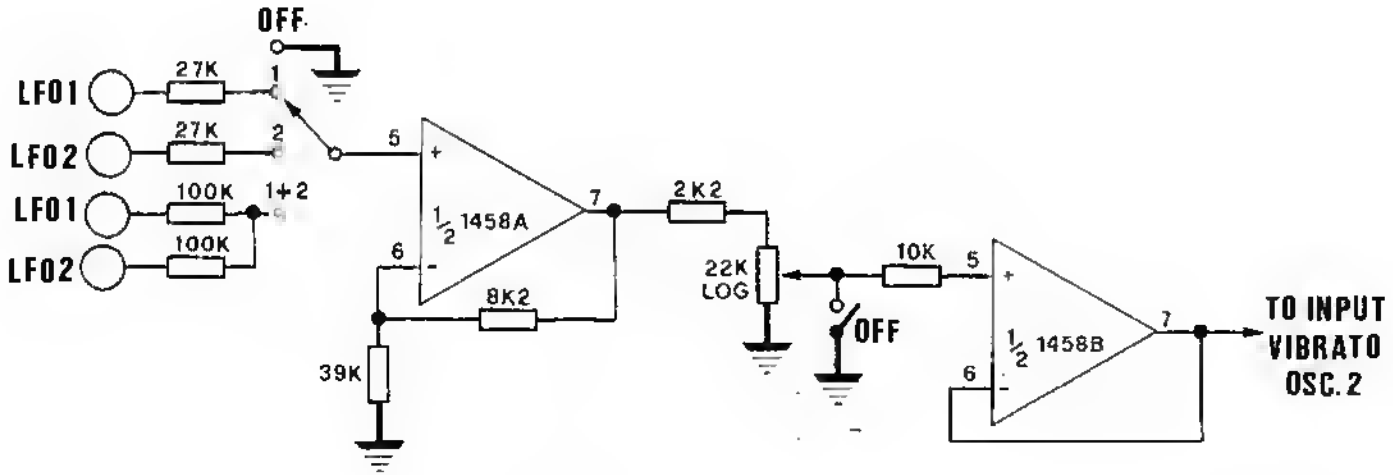
PIN	REFERENCE J1	PIN	REFERENCE J2
1	+12V	1	OUT ADSR VCF
2	−12V	2	
3	R POT	3	
4	S POT	4	+5V
5	GND	5	R POT
6	GND	6	S POT
7	GND	7	GND
8	GND	8	GND
9	D POT	9	GND
10	A POT	10	GND
11	GATE	11	D POT
12	OUT ADSR VCA	12	A POT

MODEL DS DS SCHEMA L			REVISION	-		
DATE	DRAWN BY	DESIGNED BY	DATE			

DWG 7







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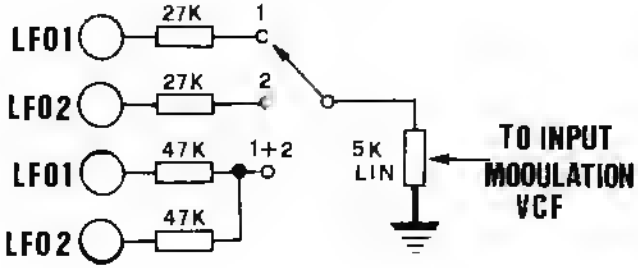
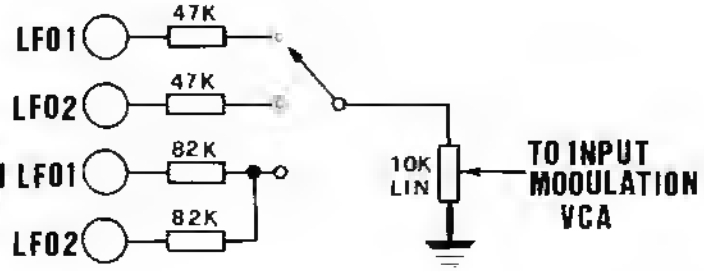
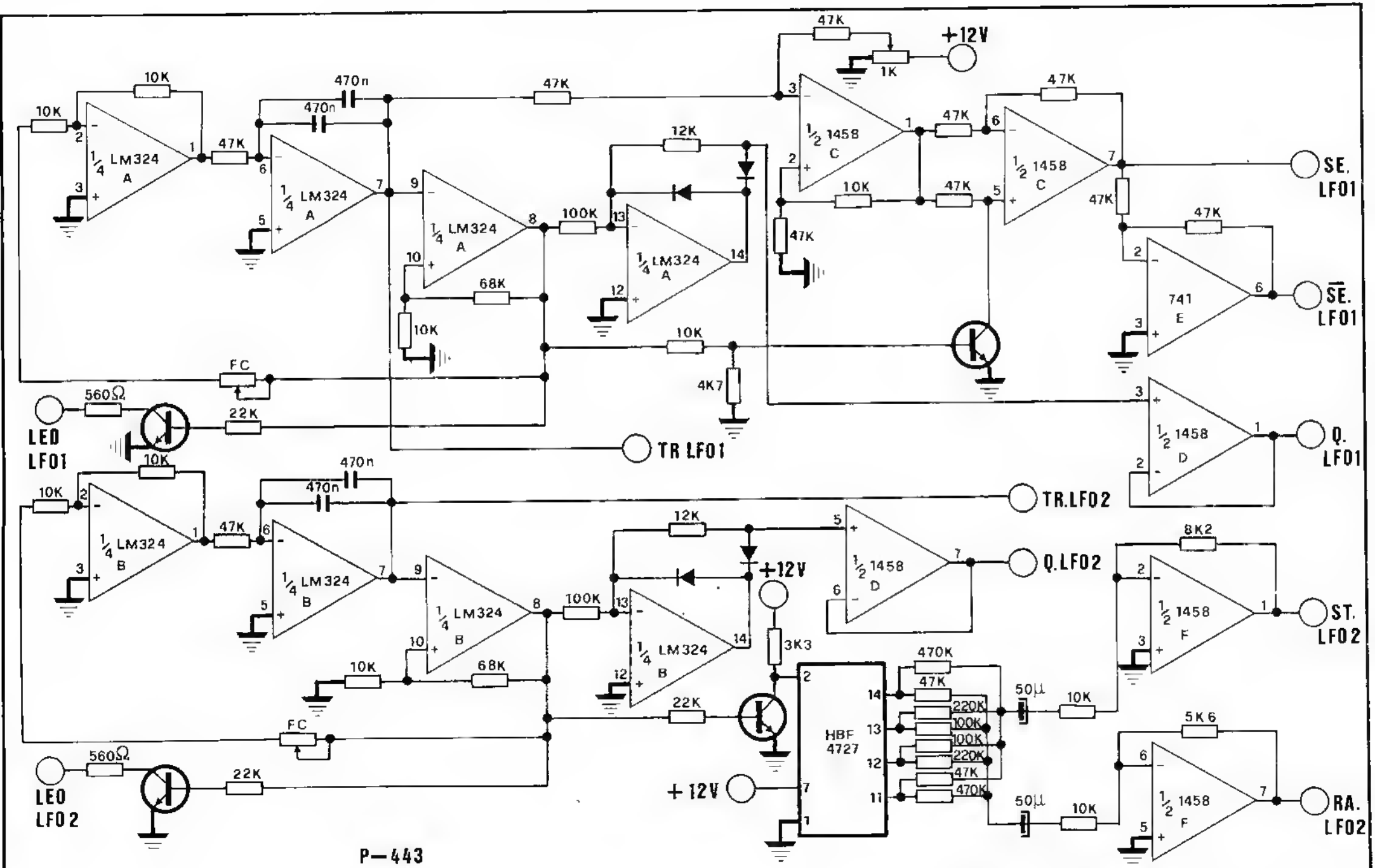




MODEL DS2 SCHEMA M			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			



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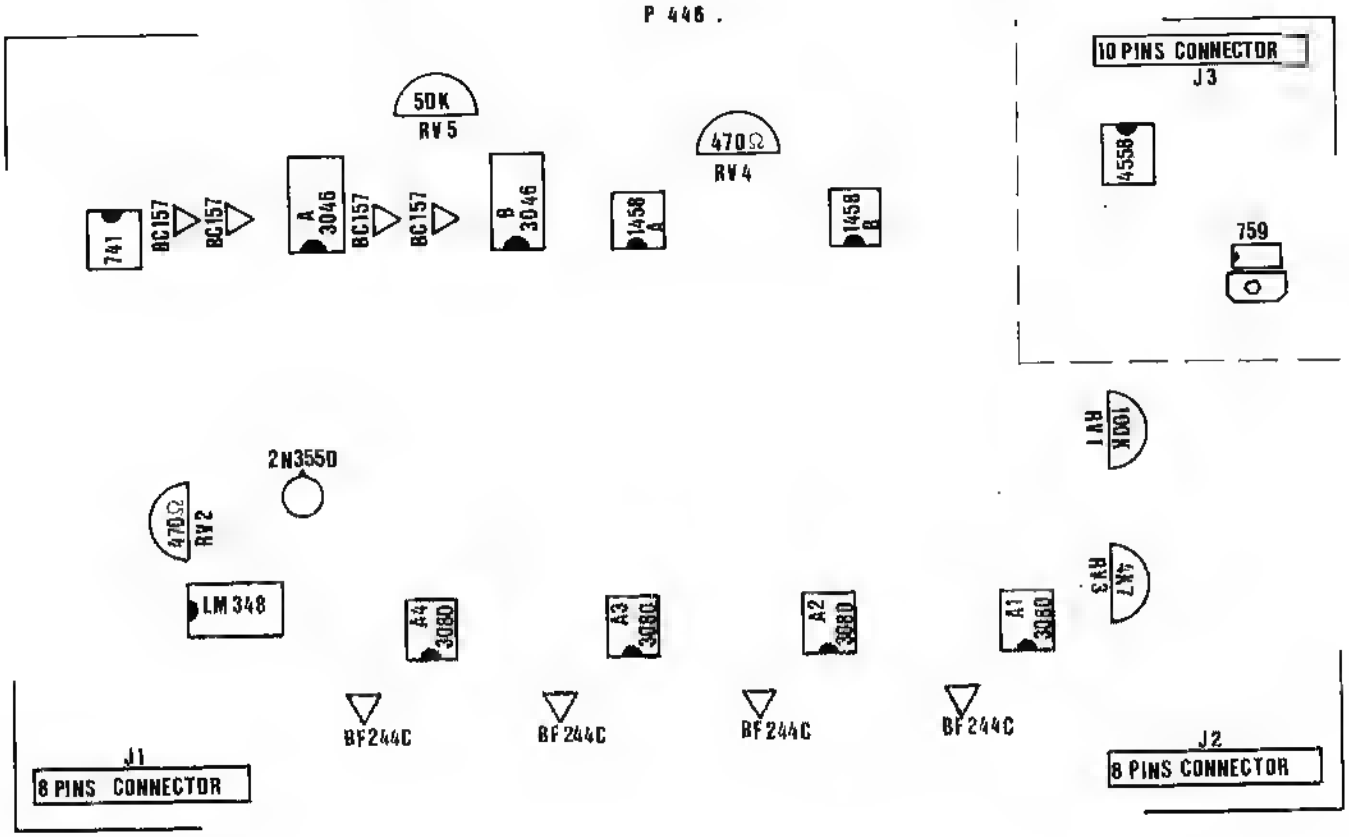
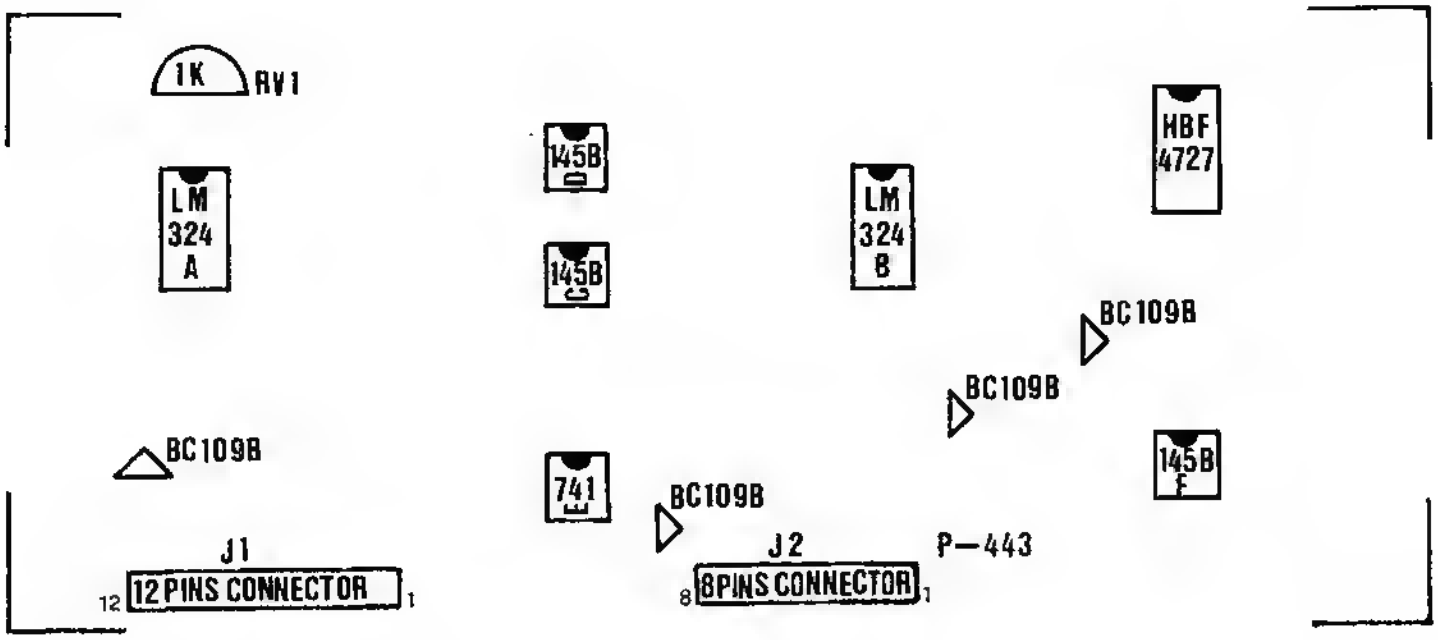
MODEL	DS2 SCHEMA N	REVISION			
DATE	DRAWN BY Bordwin	DESIGNED BY R Braun	DATE		

DWG 9



PIN	REFERENCE J1	PIN	REFERENCE J2	PIN	REFERENCE J3
1	−5.6V	1 2	GND	1	ADSR VCA
2	CUTOFF POT	3	RESON CENTR.	2	MODULAT INPUT
3	GND	4	POLY	3	−12V
4	MODULAT INPUT	5	NOISE	4	+12V
5	ADSR VCF	6	OSC 1	5	GND
6	KT SW TA	7	OSC 2	6	GND
7	RESONANCE LATER.	8		7	OUT VOL GEN
8	GND			8	INPUT HEAD PH
				9	GND
				10	OUT HEAD PH

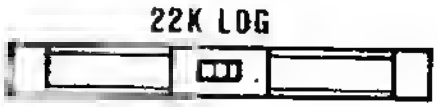


PIN	REFERENCE J1
1	SE. LFO1
2	SE. LFO1
3	QUAORA LFO1
4	FC LFO1
5	−12V
6	TRI. LFO1
7	GNO
8	"
9	"
10	LEO LFO1
11	FC LFO1
12	+12V

PIN	REFERENCE J2
1	STAIRCASE
2	"
3	SeH
4	LEO LFO2
5	FC LFO2
6	QUAORA LFO2
7	TRI. LFO2
8	FC LFO2

MODEL	DS2 SCHEMA N		REVISION			
DATE	DRAWN BY Bordai G.	DESIGNED BY R Boran	DATE			

DWG11



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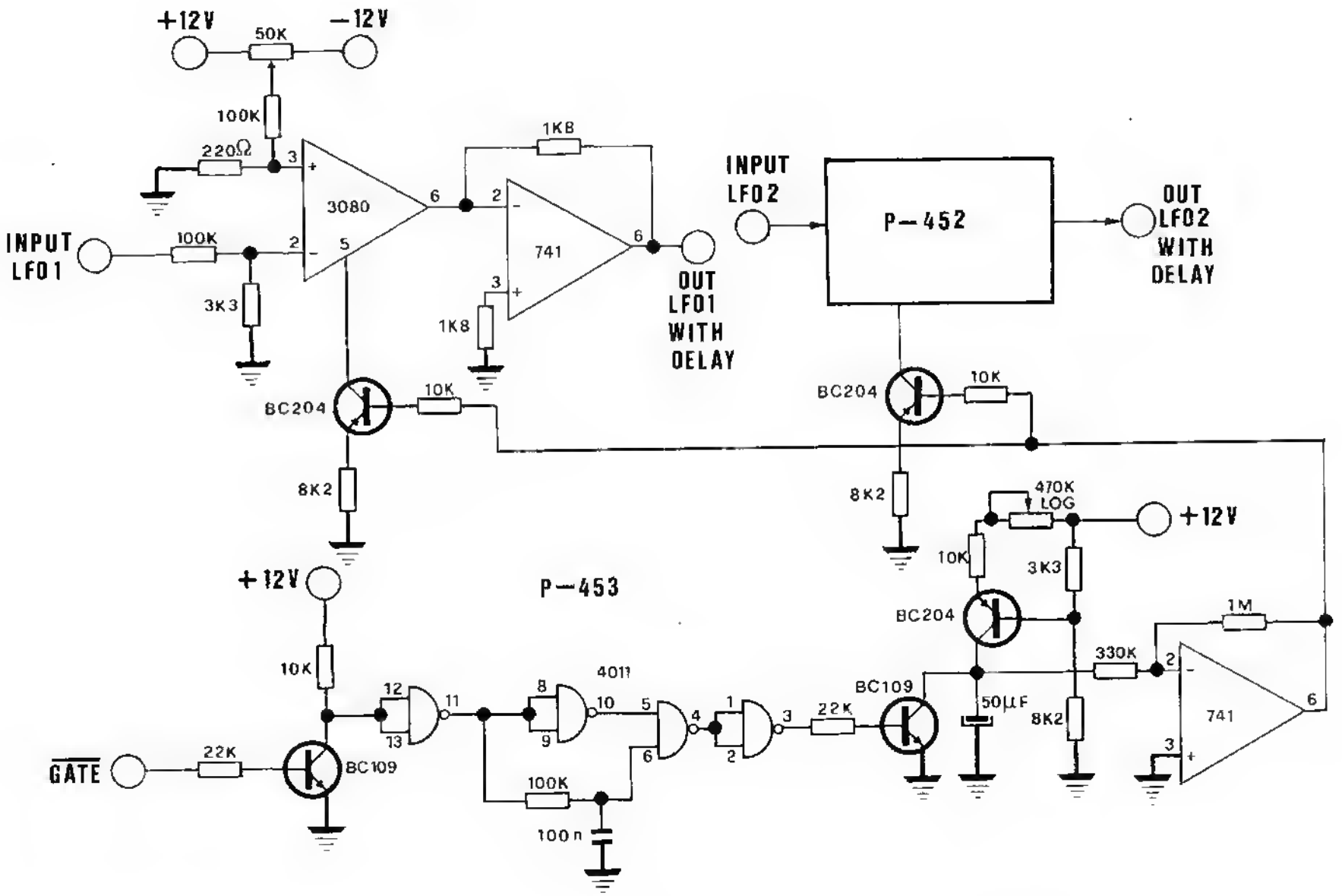
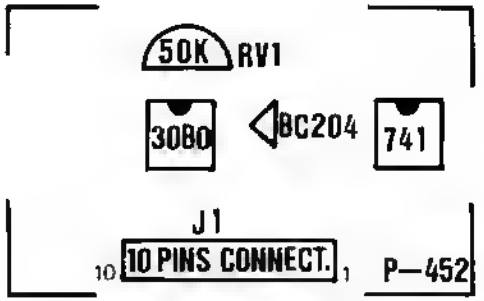
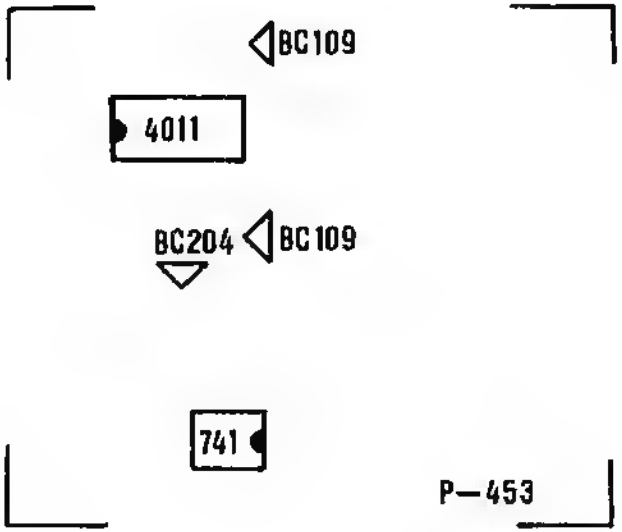
MODEL	DS2 SCHEMA M		REVISION			
DATE	DRAWN BY Bardani G.	DESIGNED BY R Bardani	DATE			

DWG12



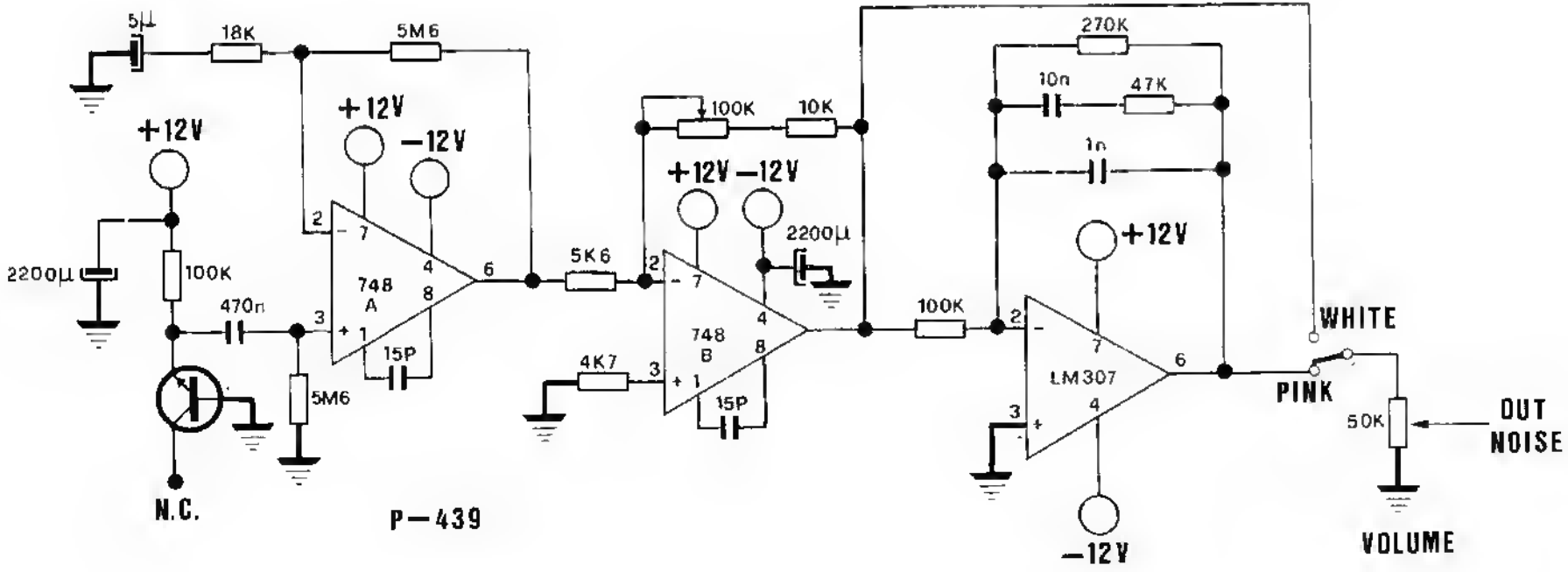
MODEL	DS2 SCHEMA O	REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE		



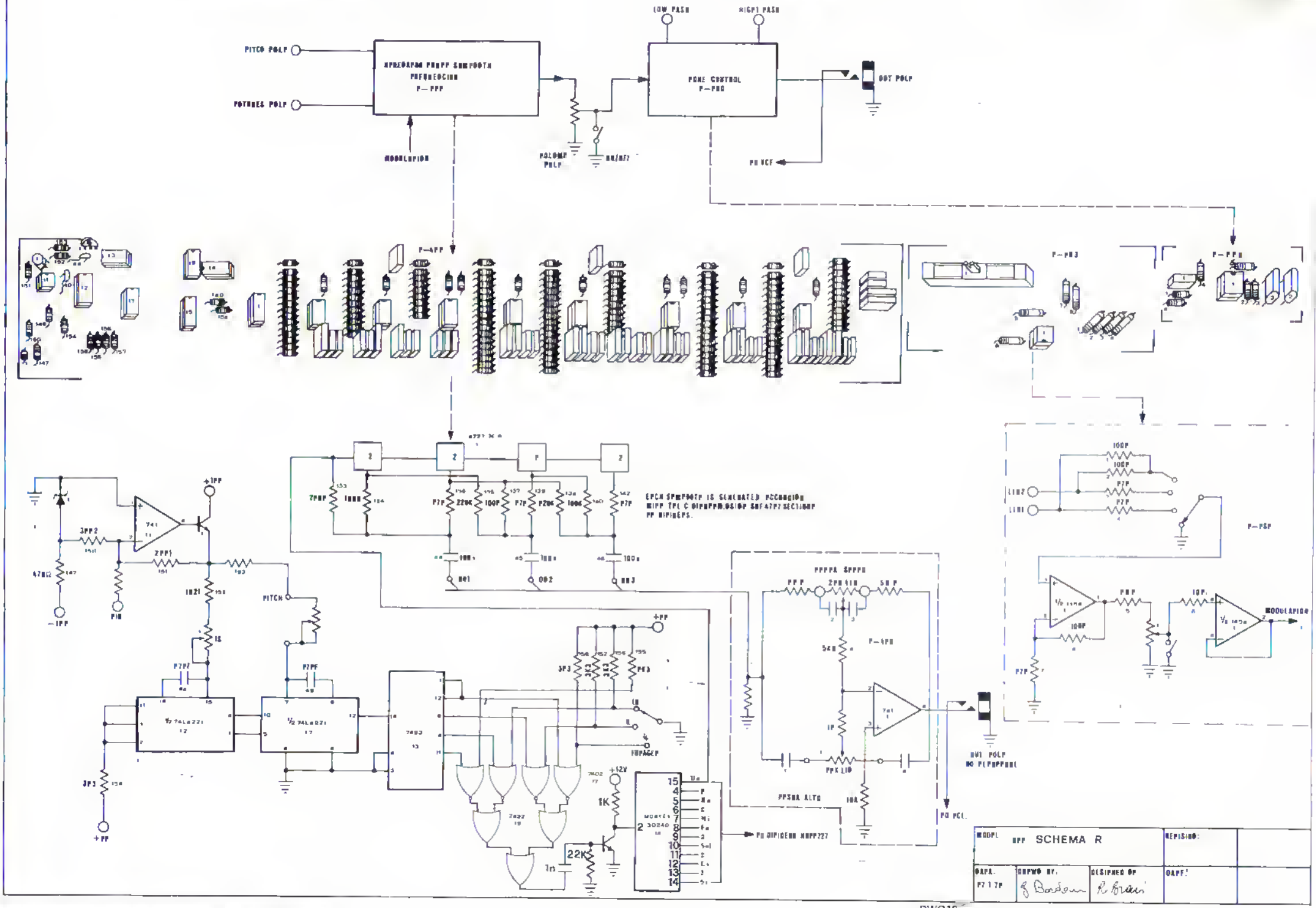


PIN	REFERENCE J1
1	+12V
2	OUT LFO1 or LFO2 WITH DELAY
3	PIN 6 741
4	−12V
5	GND
6	"
7	"
8	INP. LFO1 or LFO2
9	" " " "
10	" " " "

MODEL	DS2 SCHEMA Q		REVISION			
DATE	DRAWN BY BordaiG.	DESIGNED BY R.Borai	DATE			

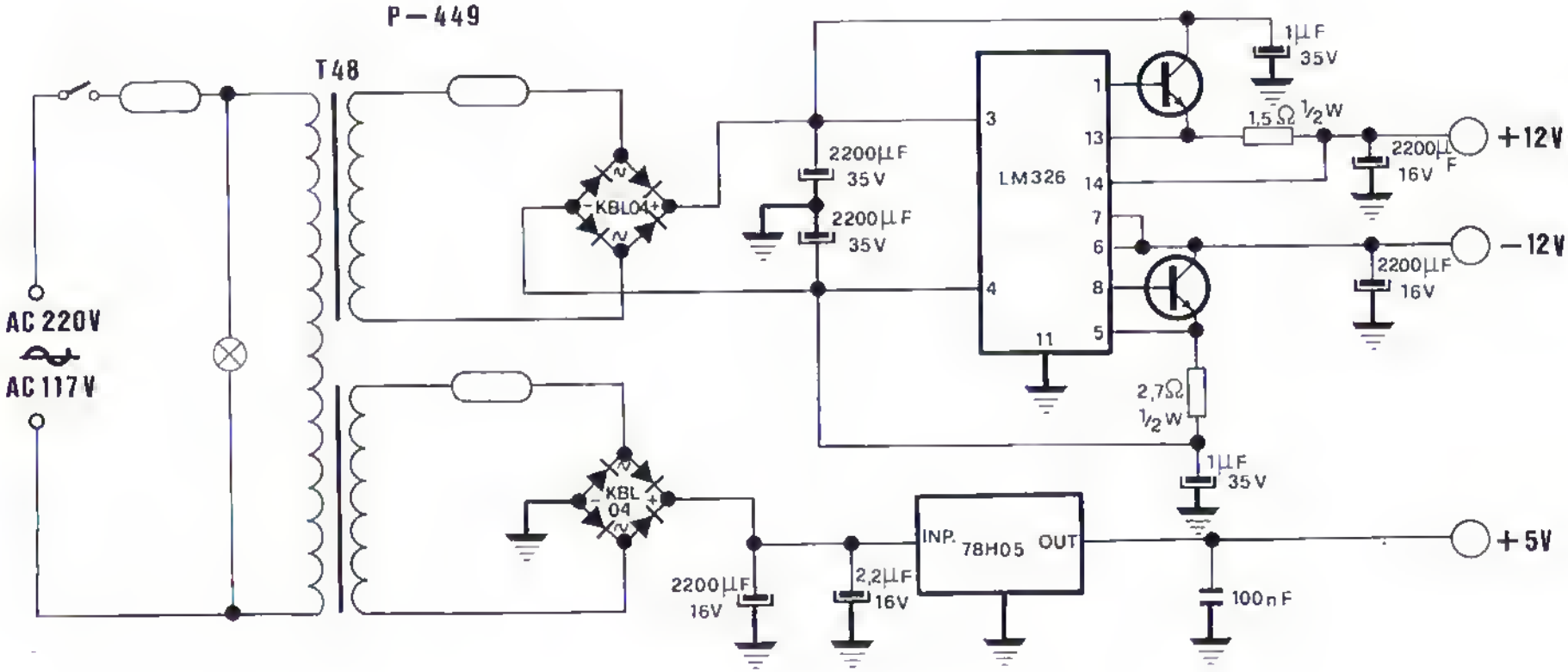


MODEL DS1	DS2 SCHEMA O	REVISION			
DATE	DRAWN BY Bordini G.	DESIGNED BY R. Brun	DATE		



MODPL PPP SCHEMA R			REPISIBO:
DAPA. P7 1 7P	DRPWO BY: J Bordeau	DESIPNED OP R Brun	DAPF:

DWG16



MODEL	DS 2 SCHEMA P		REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			

LM
326

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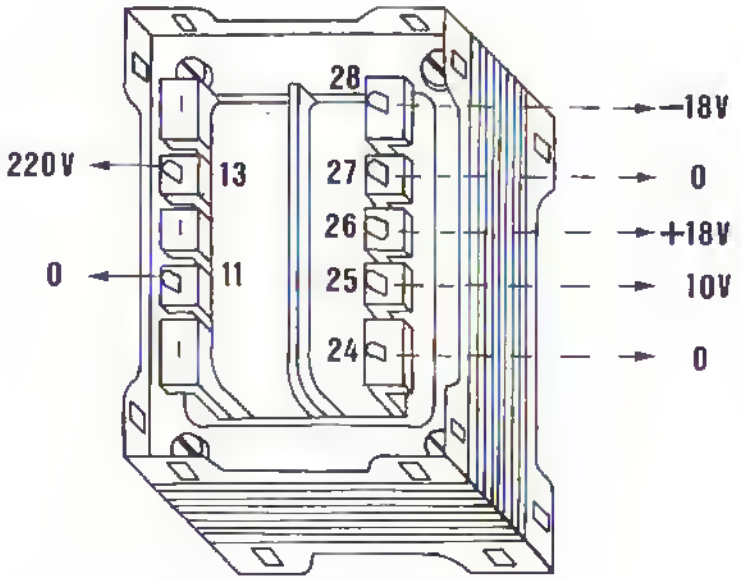

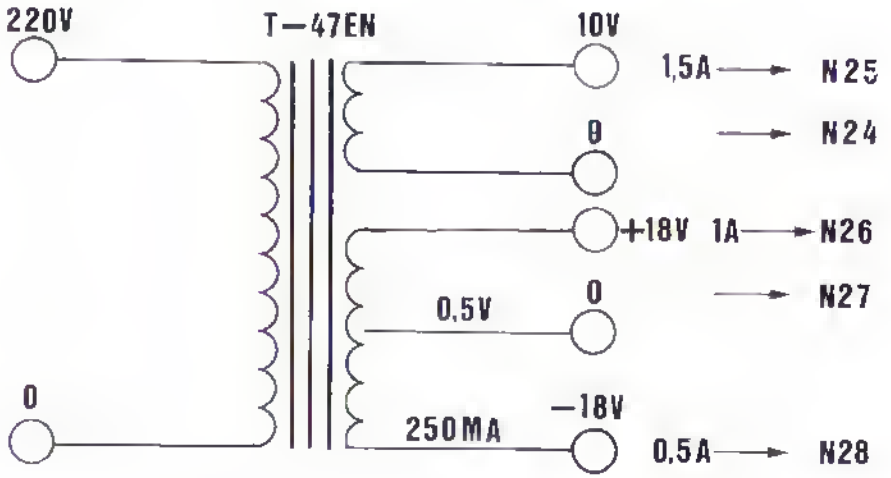

MODEL	DS 2 SCHEMA P		REVISION			
DATE	DRAWN BY Bordoni G.	DESIGNED BY R Brai	DATE			